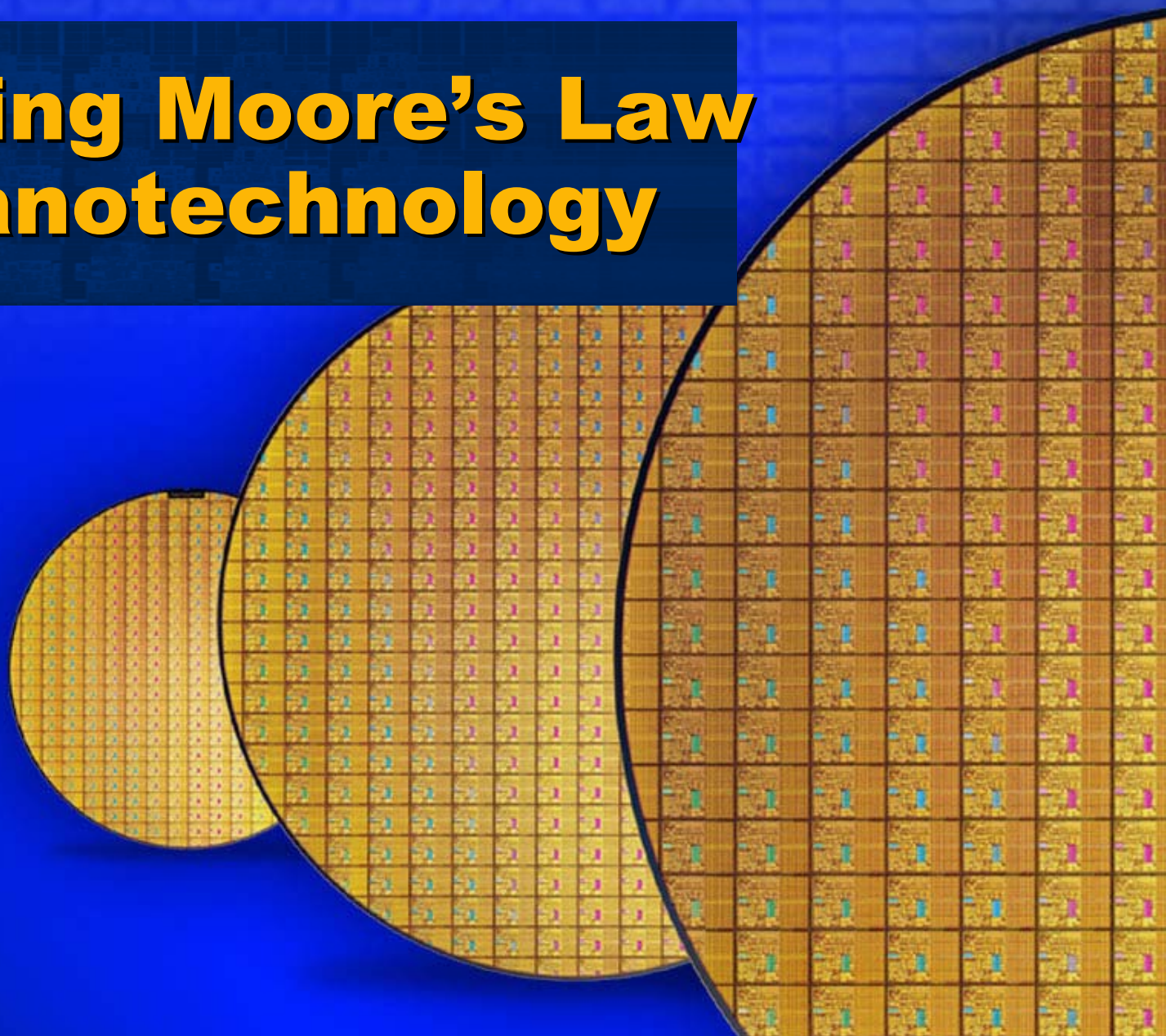
Extending Moore's Law with Nanotechnology



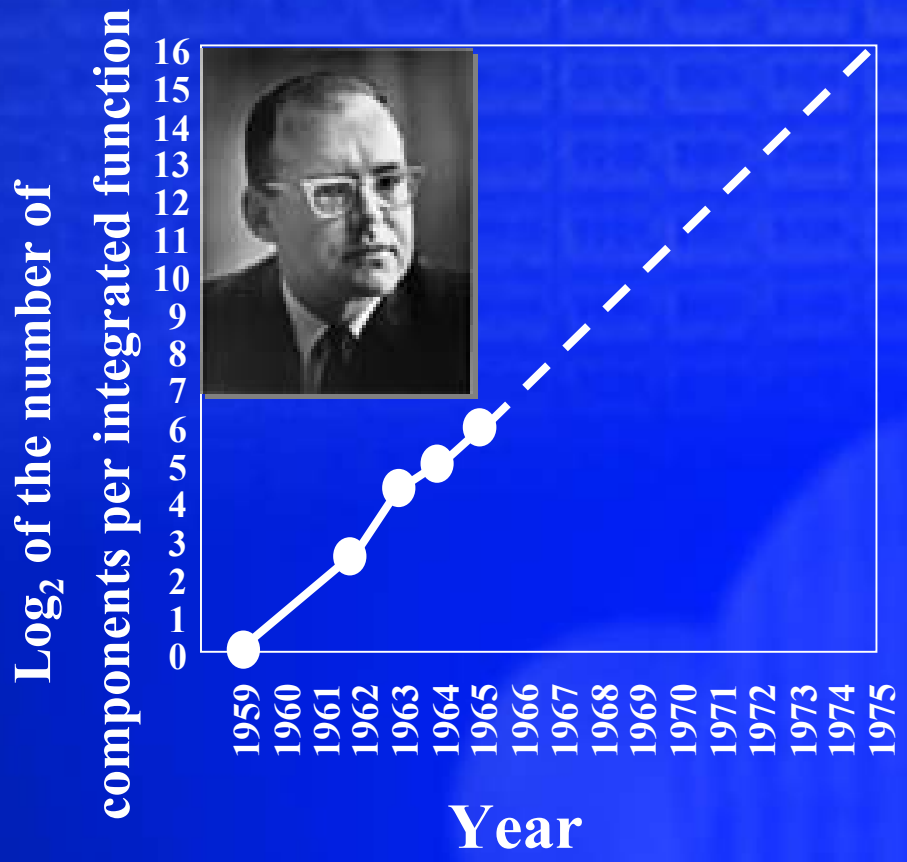
September 2003
Carolyn Block, PhD
Senior Staff Engineer
Components Research
Intel Corporation

intel

Agenda

- Historical motivations for scaling
- Si Research at Intel
  - Logic Technology Development
  - 90 nm Technology Results
- Extending technology using Moore's Law
  - Technical Criteria / Key Challenges
  - Research Directions: high K, trigate, nanotubes....
- What comes next?
- Summary

Birth of Microelectronics: Moore's Law

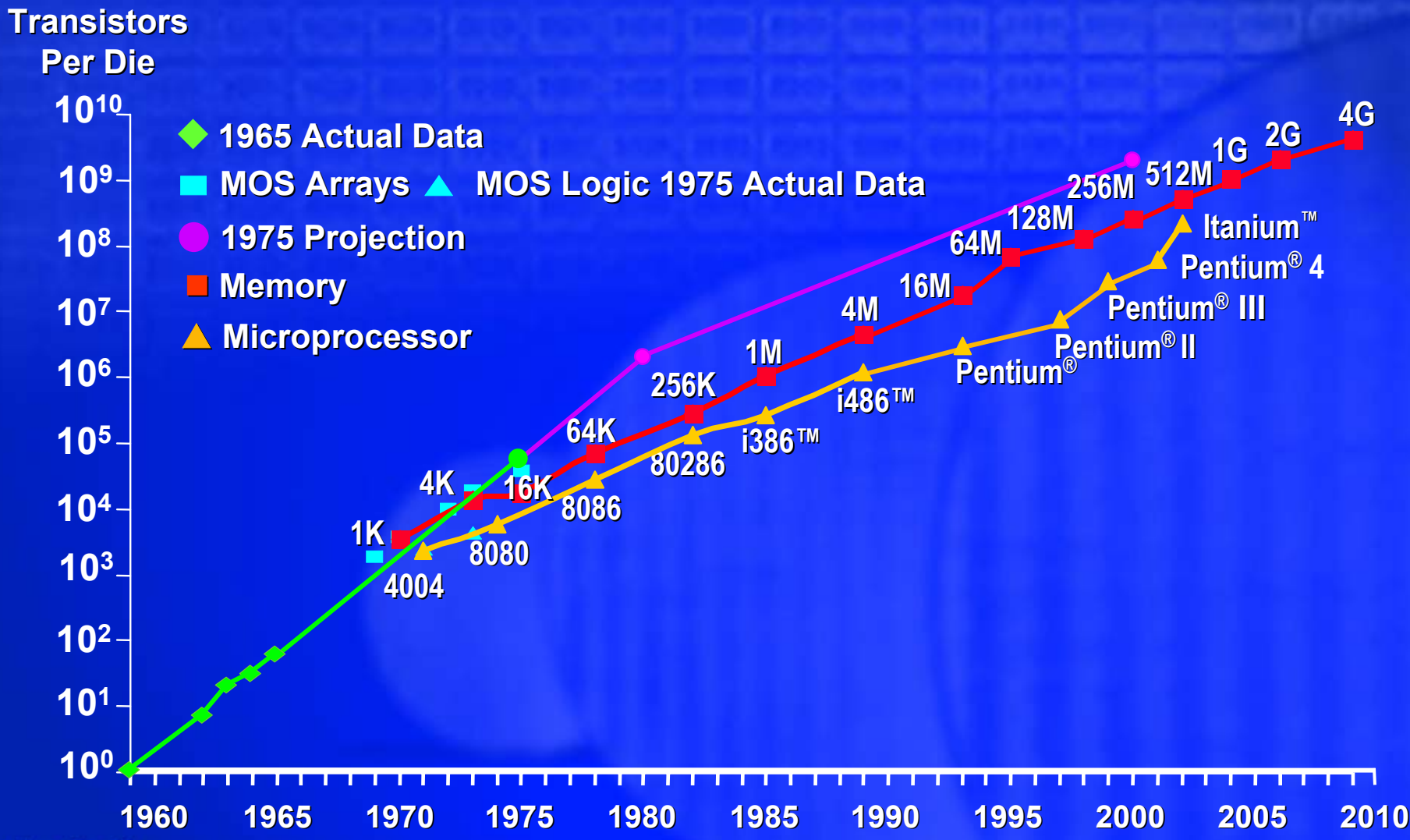


"Reduced cost is one
Of the big attractions of
Integrated electronics, and
The cost advantage continues
To increase as the technology
Evolves toward the production
Of larger and larger circuit
Functions on a single
semiconductor substrate."

"Dr.Gordon E.Moore is one of the new breed of electronic engineers, schooled in the physical sciences rather then in electronics."

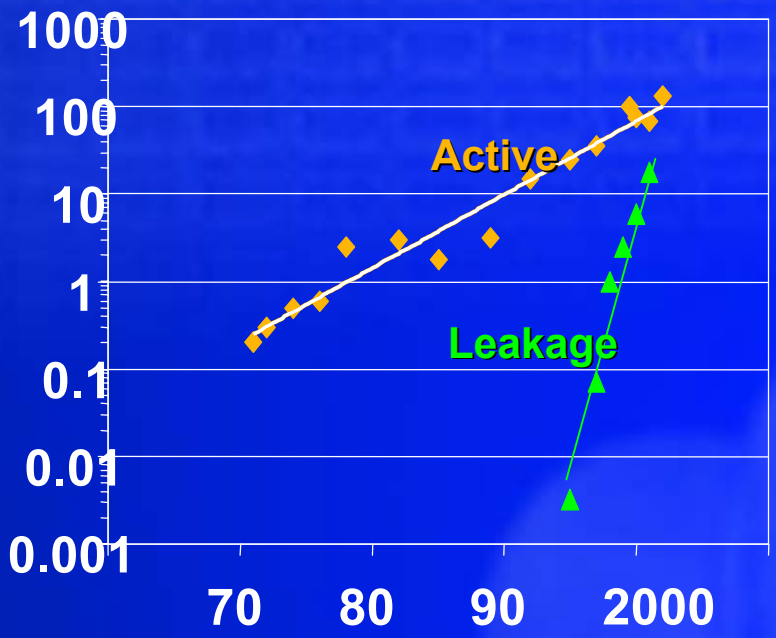
Electronics Magazine (35th anniversary), April 19, 1965

Moore's Law continues to be the benchmark

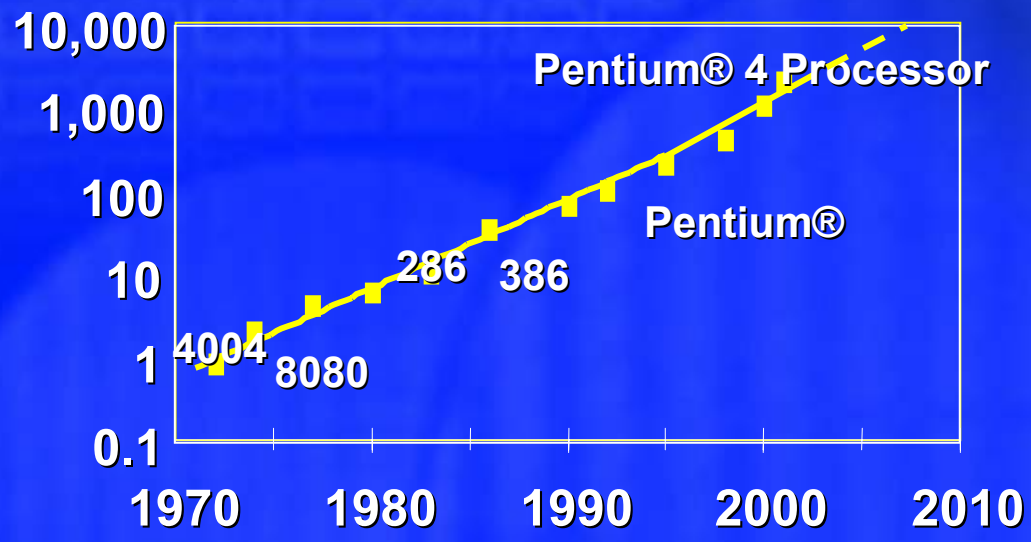


Source: Intel

Effects of Scaling



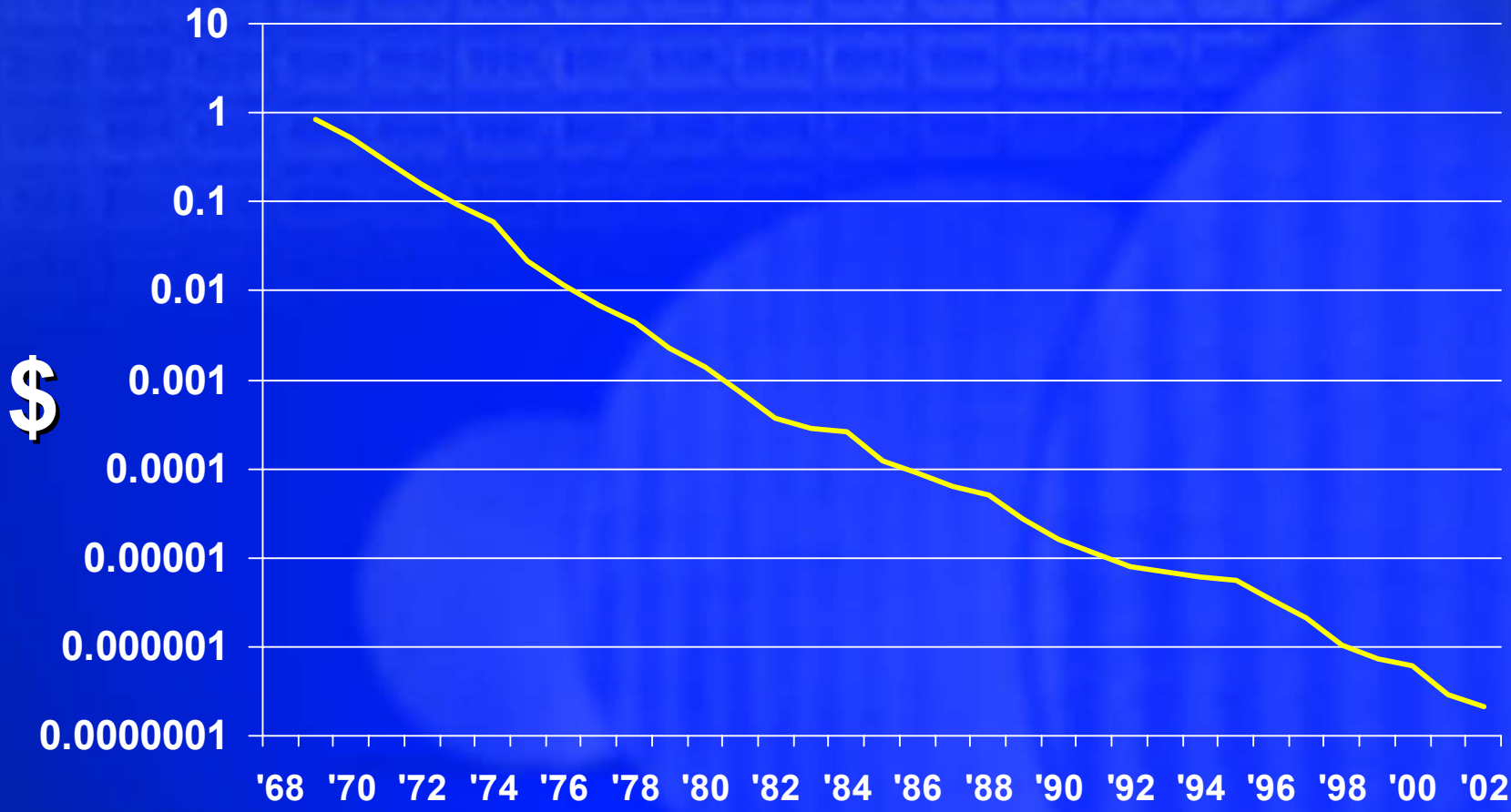
Power (Watts)



Clock Frequency (MHz)

intel

Effects of Scaling: Cost



Source: WSTS/Dataquest/Intel, 8/02

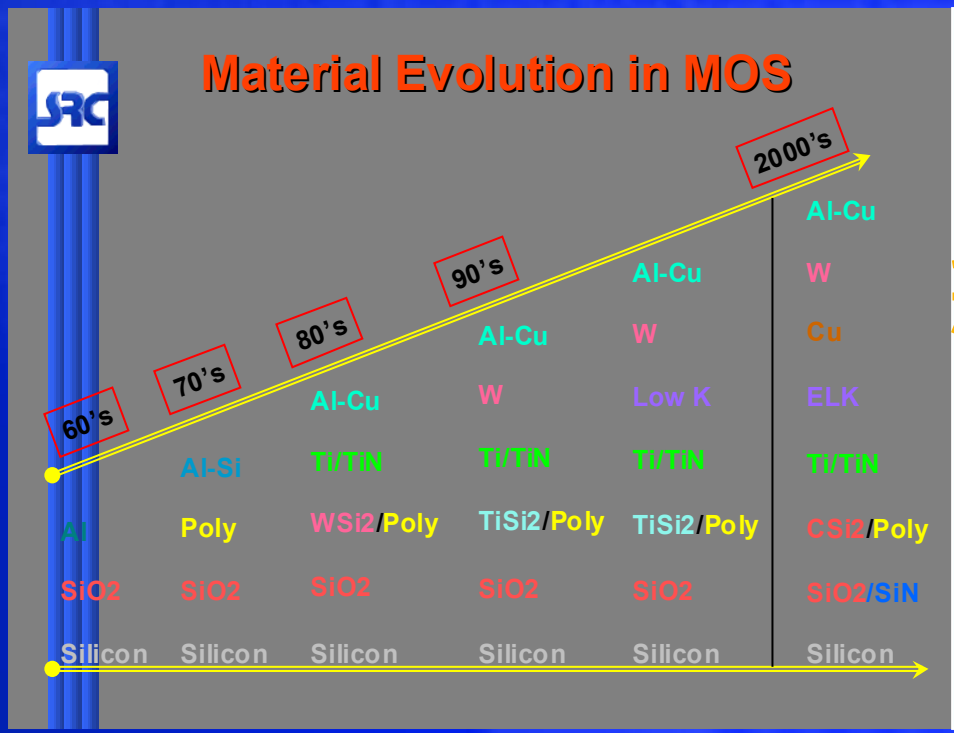
The beauty of silicon

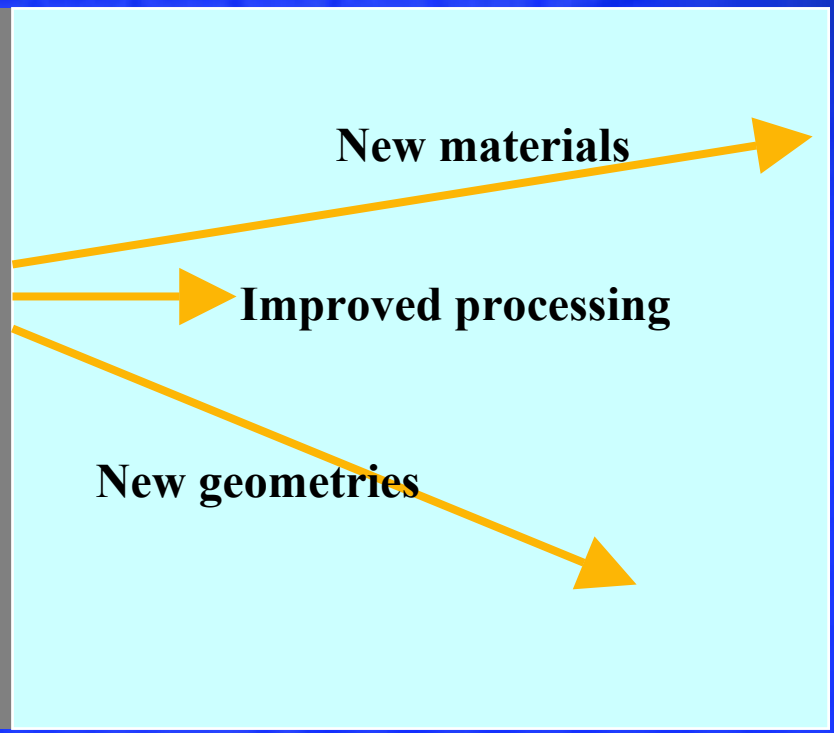
For four decades, the semiconductor industry has steadily reduced the unit cost of IC components by

1. Scaling device dimensions downward
2. Scaling wafer diameter upward

	1990	1995	2000
DRAMs	**4 MB**	**64 MB**	**1 GB**
Feature size	**0.8 µm**	**0.35 µm**	**0.15 µm**
Wafer diameter	**6”**	**8”**	**12”**
Cost per Megabit	$6.50	$3.14	$0.10

The ingredients of scaling





Scaling Will continue as long as
(δ cost) /(δ performance) < alternate technologies

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- What comes next?
- Summary

Silicon Research at Intel

- Logic Technology Development (OR, CA, AZ)
  - Lithography, Transistors, Interconnects, Packaging, Environmentally Benign Materials
- Non-Volatile Memory
  - Ovonics (CA)
  - Polymers (OR)
- Opto-electronics (CA)
- MEMS (CA)
- Biotechnology (CA)

Production, Development and Research Synergy

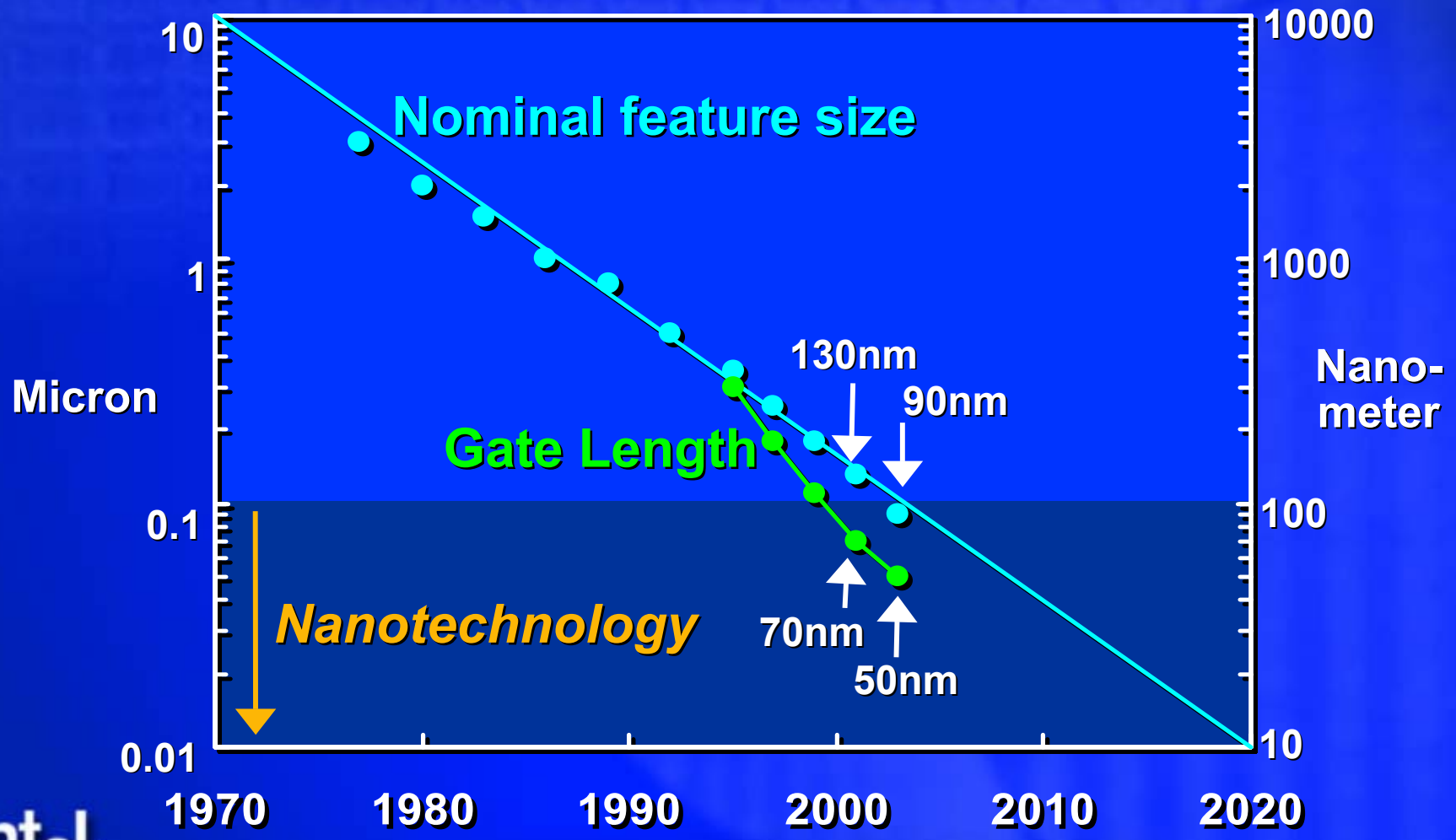
F20: 200mm
130 nm Production

D1C: 300mm,
130nm Production
90nm Development

RP1: 300mm
Research

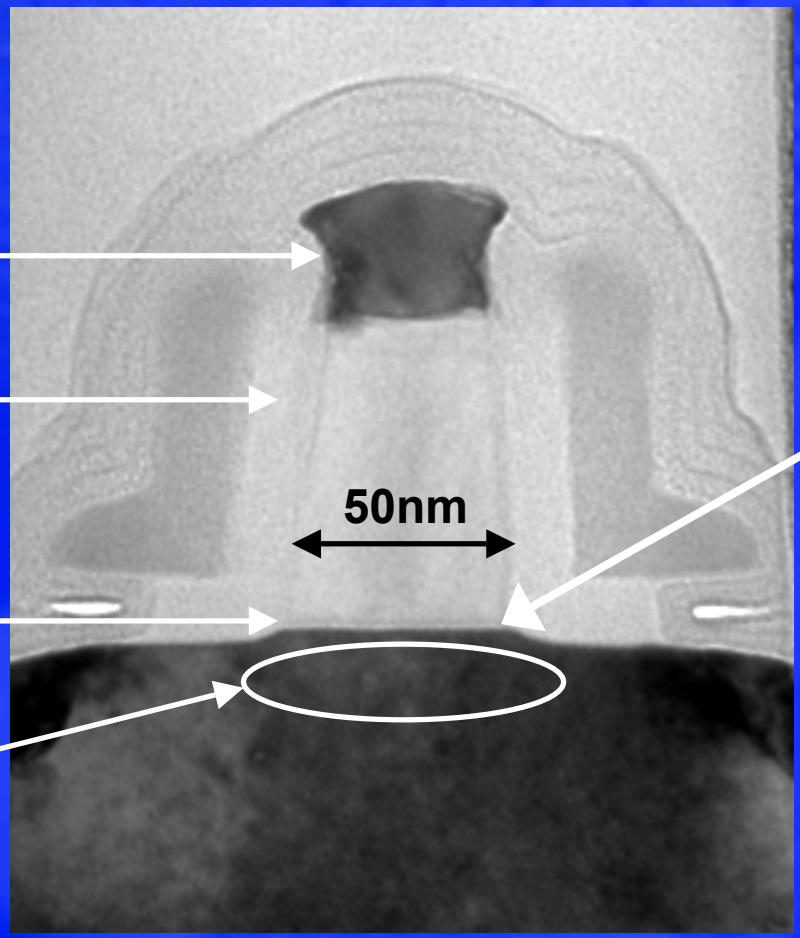
D1D: 300mm
65 nm Development

Intel in Production with Nanotechnology (< 100nm)



90nm Logic Technology

90 nm Generation Transistor



Silicide Layer

Silicon Gate Electrode

1.2 nm SiO_2 Gate Oxide

Strained Silicon

Future Options

gate loop engineering

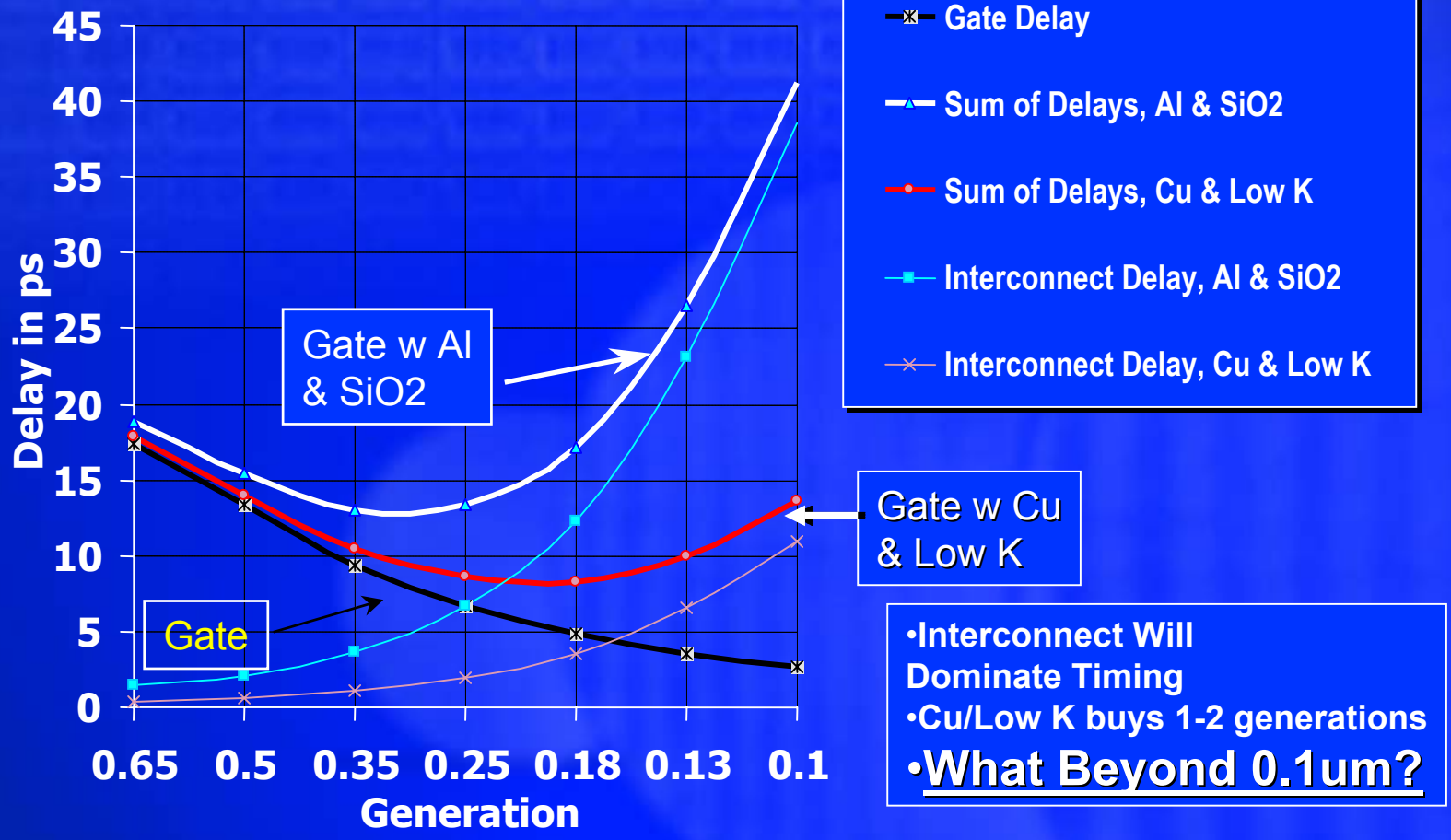
New transistor structure

Source: Intel

50 nm L_{GATE} + 1.2 nm Oxide + Strained Silicon
for industry leading transistor performance

intel

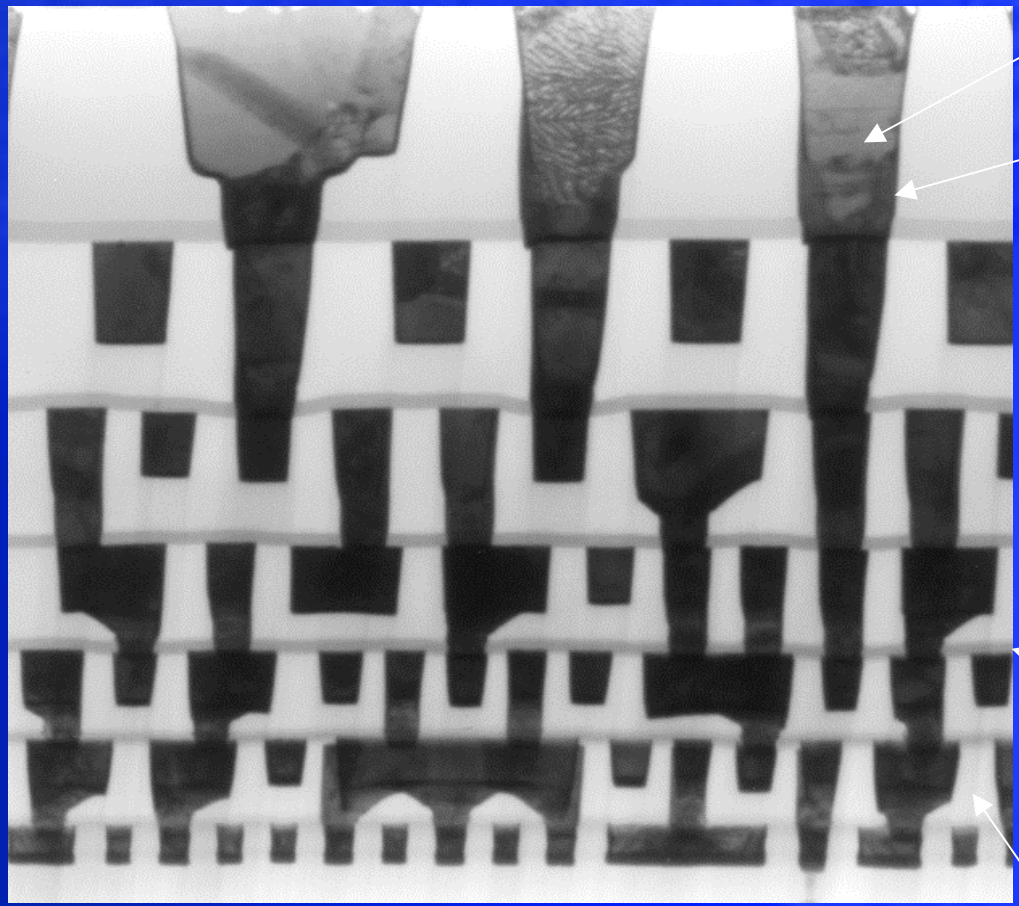
Interconnect Challenges: Delay



- Interconnect Will Dominate Timing
- Cu/Low K buys 1-2 generations
- **What Beyond 0.1um?**

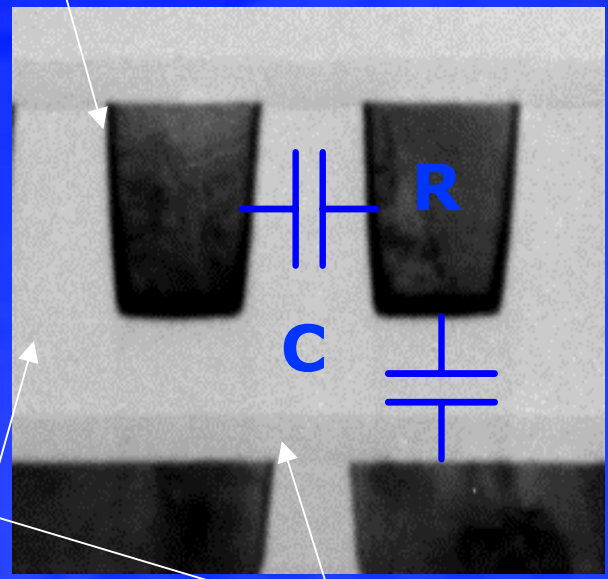
Data From: Bohr, Mark T; "Interconnect Scaling -The Real Limiter to High Performance ULSI"; Proceedings of the 1995, IEEE International Electron Devices Meeting; pp241-242

90nm Interconnects



copper interconnects

thin barriers



etch stop

low K dielectrics

intel

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How do we continue to drive Moore's Law?

- CMOS scaling will continue for > 10 years
  - Si CMOS + New Materials
  - Dielectrics and Gate
  - Interconnect
  - Channel
- Nanoscience research is needed to facilitate radical new scalable technologies in the future
  - Need to identify most promising options (materials, processes, structures)
  - Must utilize silicon technology's foundation

intel

Technical criteria

- *CMOS compatibility*
- *Energy efficiency*
- *Scalability*
- *Performance*
- *Architectural compatibility*
- *Sensitivity to parametric variation*
- *Room temperature operation*
- *Stability and reliability*

"No exponential lasts forever but we can delay forever"

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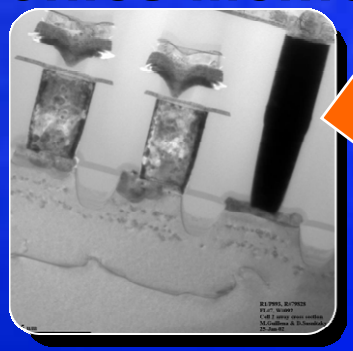
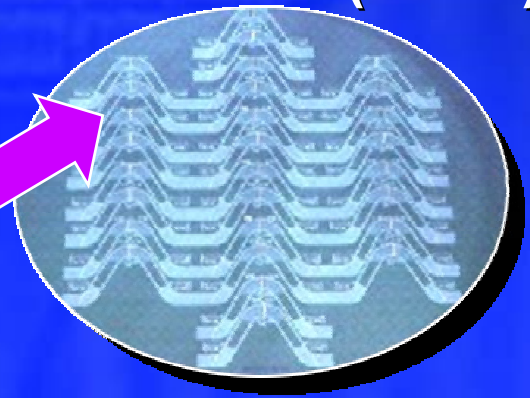
Adaptable and Versatile Silicon Technology

Ovonics Memory

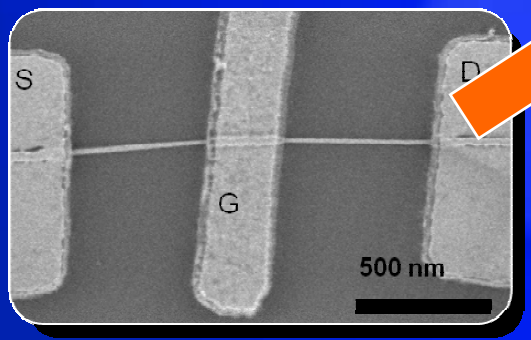


Photonics (AWG)

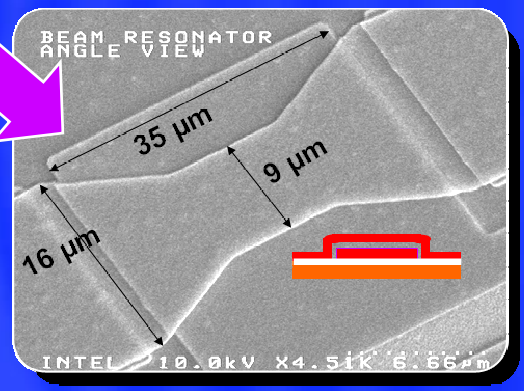


Silicon Technology Base

Nanotube/Nanowire Transistors



MEMS for RF



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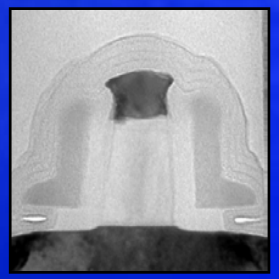
Key Challenges to Scaling

- Transistor
  - Gate Oxide Leakage
  - Source-drain leakage
  - Short Channel Performance
  - Vcc scaling
- Patterning
- Interconnects, Packaging
  - RC delay
  - Power delivery, distribution
  - Thermal Management

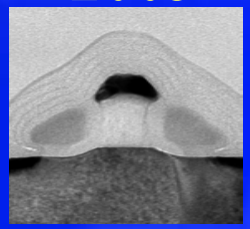
Intel Nano Transistors

90nm Node
2003



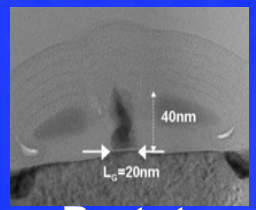
50nm Length (IEDM2002)

65nm Node
2005



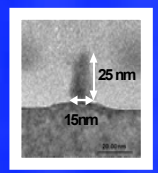
30nm Prototype[1]

45nm Node
2007



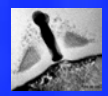
20nm Prototype[2]

32nm Node
2009



15nm Prototype[3]

22nm Node
2011



10nm Prototype[4]

References

1. IEDM, R. Chau et al., 12/00
2. 2001 Silicon Nanoelectronics Workshop, R. Chau et al., 6/01
3. TeraHertz Transistor press briefing, G. Marcyk & R. Chau, 11/01
4. 61st Device Research Conference, R. Chau et al., 6/03

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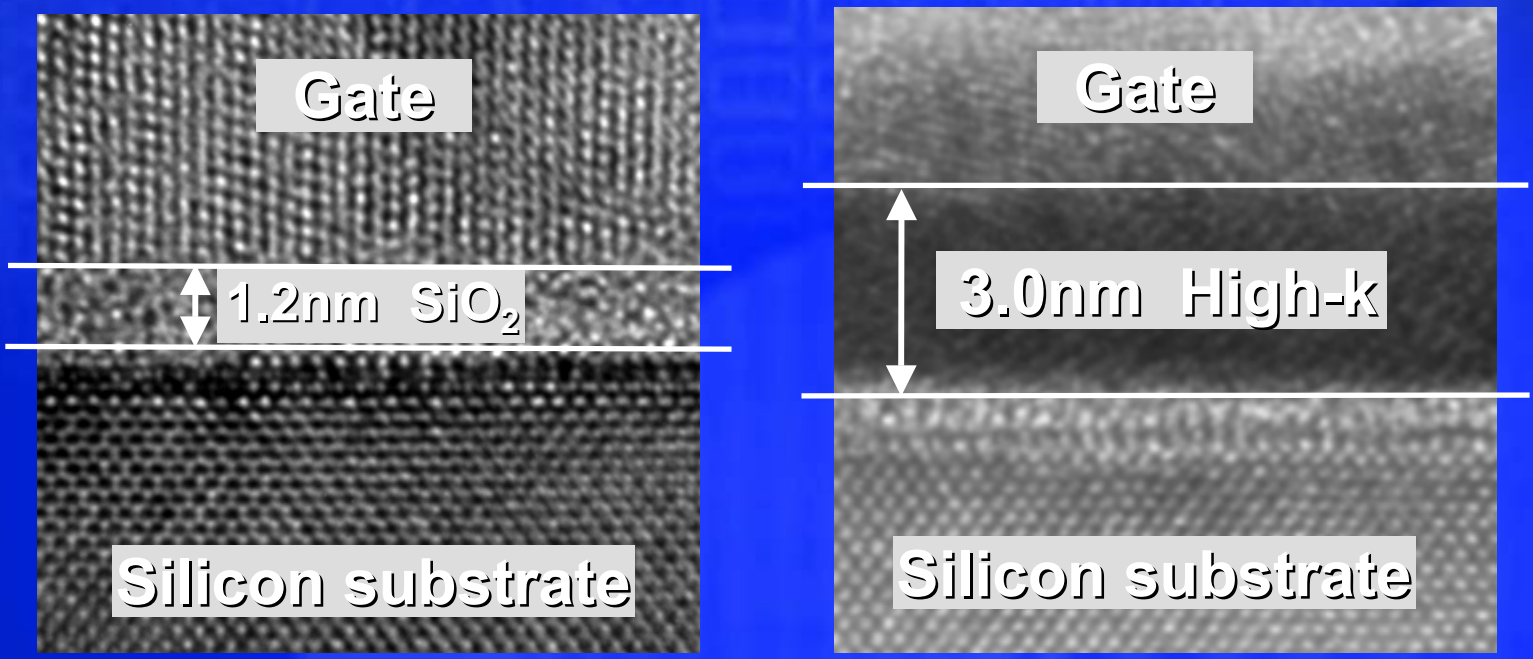
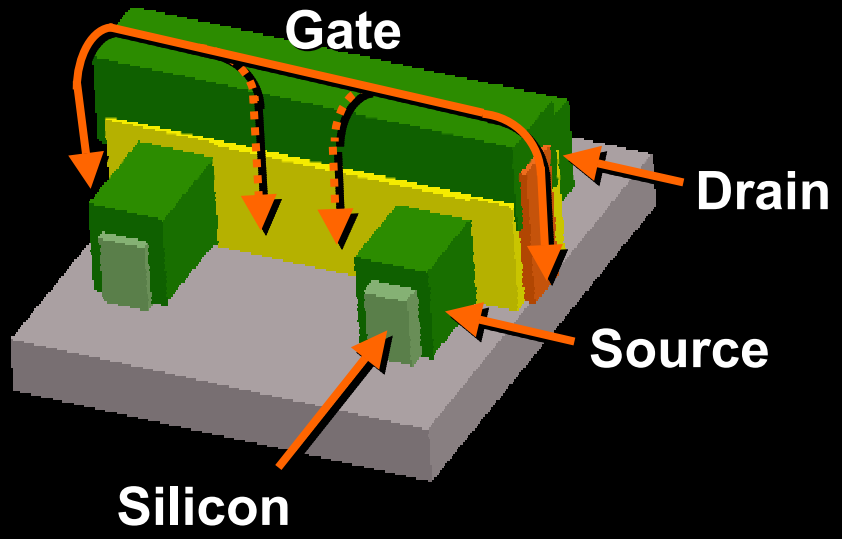
Nanotechnology for Gate Dielectrics

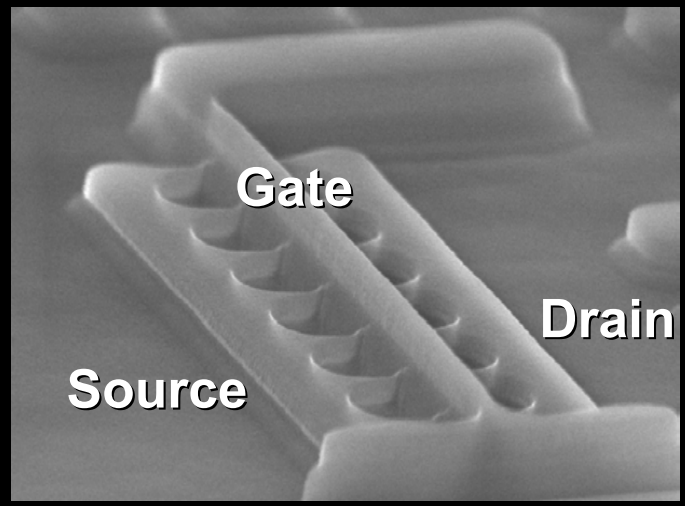


Source: Intel

	90nm process	Experimental high-k
Capacitance	1X	1.6X
Leakage	1X	< 0.01X

Experimental Tri-Gate Transistor





Source: Intel

- Improved version of TeraHertz transistor
  - Better performance
  - Scalable to smaller sizes (low leakage)
  - Possible intercept towards end of decade?

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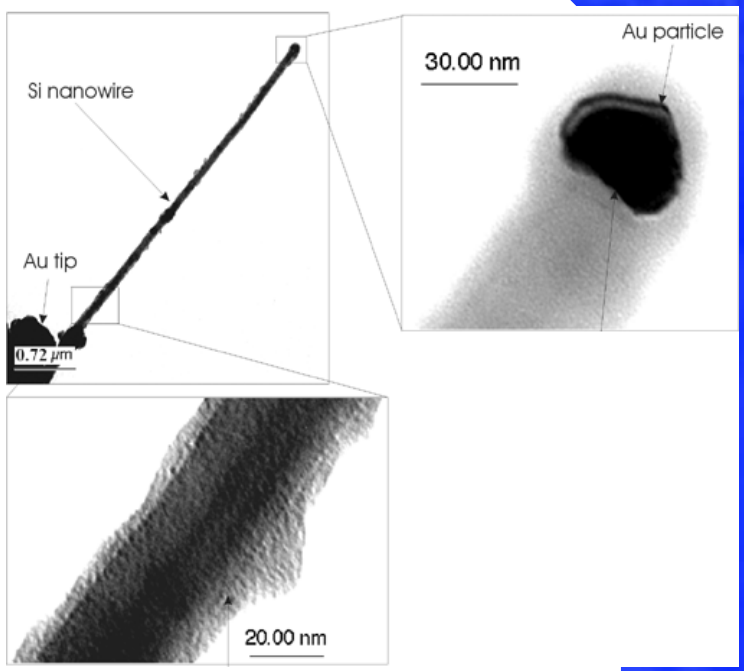
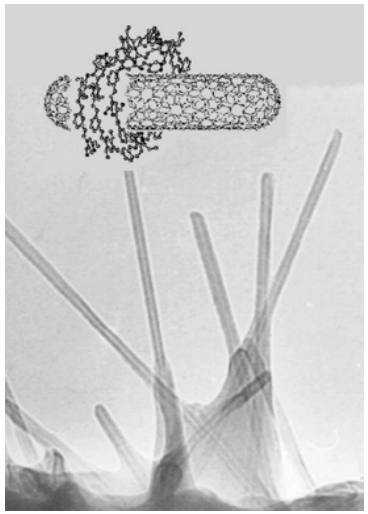
Future Nanotechnology will compliment & extend Silicon Technology

Silicon Nanowire*





Carbon Nanotube**

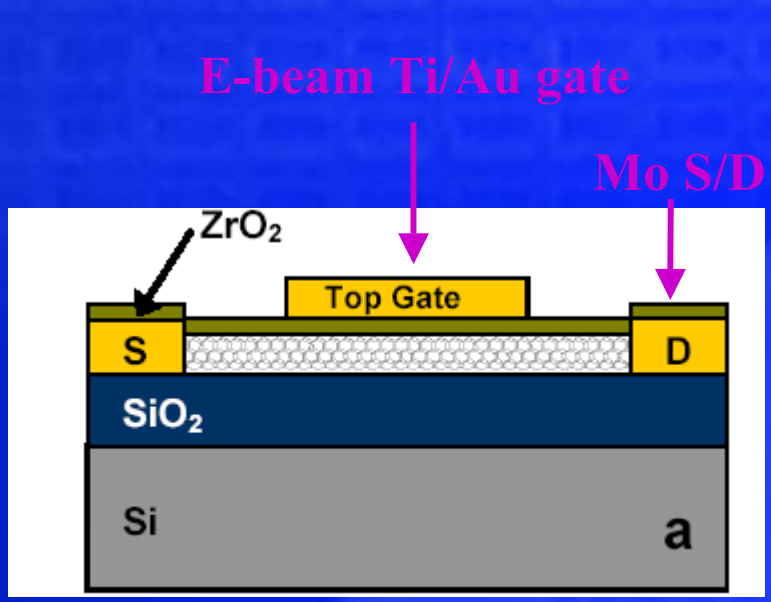
Nanotube/Nanowire Transistors

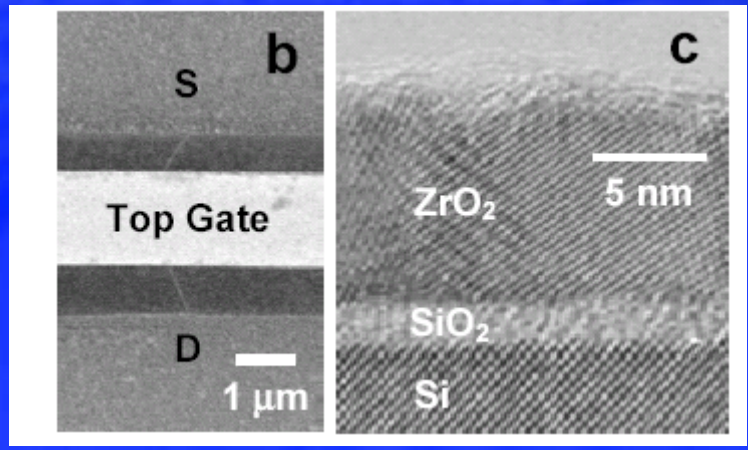
*Source: Holmes et al, University College Cork

**Source: Blau et al, Trinity College Dublin

Many options, but no clear winners…

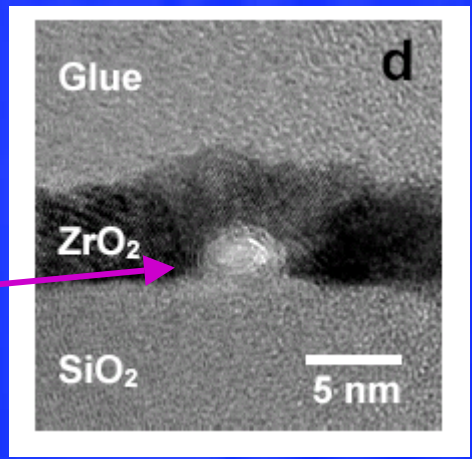
CNT-FET Device Structure





8 nm ZrO2

1.4 nm diameter single wall CNT



McEuen et. al, . Cornell Universwity

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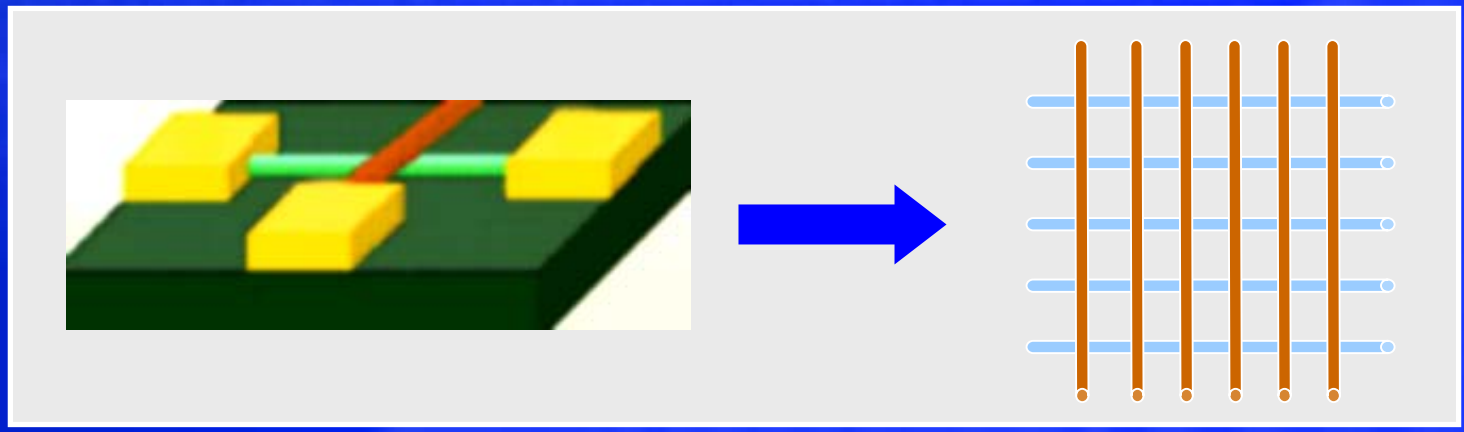
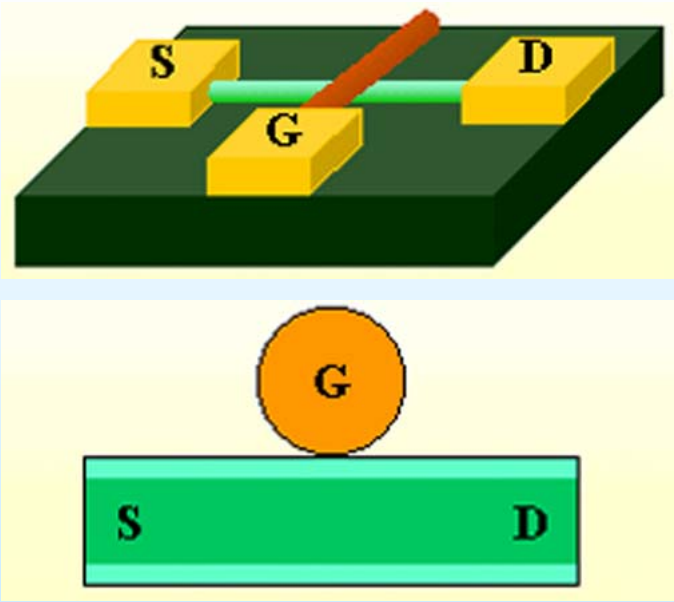
Crossed Nanowire Structures: A Powerful Strategy for Creation & Integration of Nanodevices

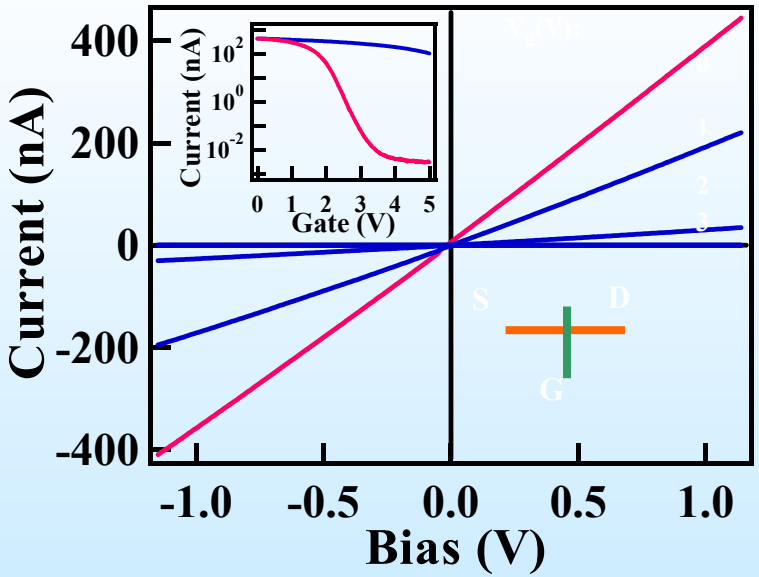


- Nanowires serve dual purpose: both active devices and interconnects.
- All key nanoscale metrics are defined during synthesis and subsequent assembly.
- Crossed nanowire architecture provides natural scaling and potential for integration at highest densities.
- No additional complexity (with added material).

C. Leiber et. al. , Harvard U

Crossed Nanowire FETs





- In crossed nanowire FETs (cNW-FET), all critical nanoscale metrics are defined by synthesis and assembly:
  - channel width by the active nanowire diameter (to 2 nm)
  - channel length by the gate nanowire diameter (to 1-2 nm)
  - gate dielectric oxide coating on the nanowires (to 1 atomic layer)
- The conductance of cNW-FETs can be changed by more than 10^5-times with less than 0.1 V variation in the nano-gate.

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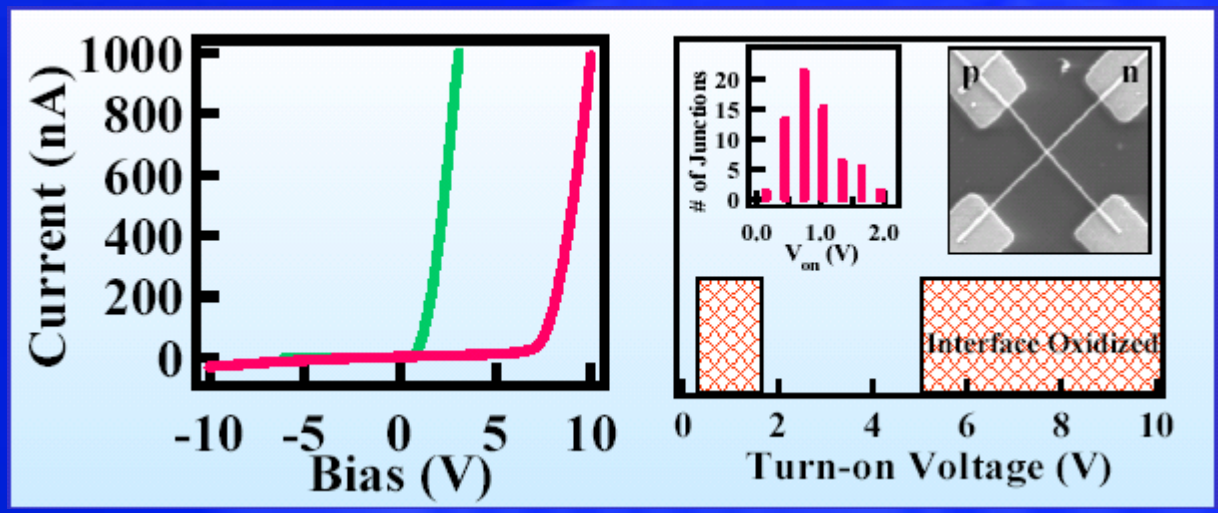
Huang, Duan, Lieber et al., *Science* **294**, 1313 (2001)

Device Demonstrated

P-N Junction



Lieber/Harvard

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Future of Nanocomputing

Scalable new technology

criteria

Scalable new technology

criteria

Silicon highway

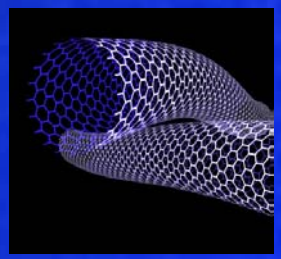
limits

characteristics

origins

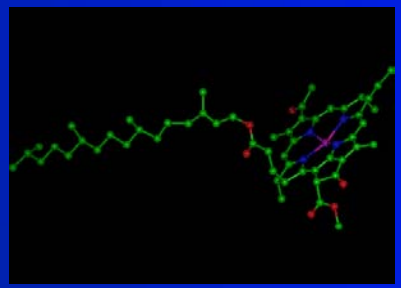
taxonomy elements

Nanotech Building Blocks

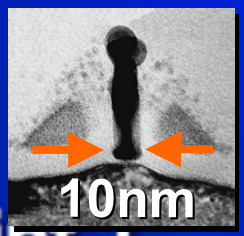


Sub 100nm particles

Molecular Assembly (directed and self assembly)



Macromolecules



Sub 100nm structures

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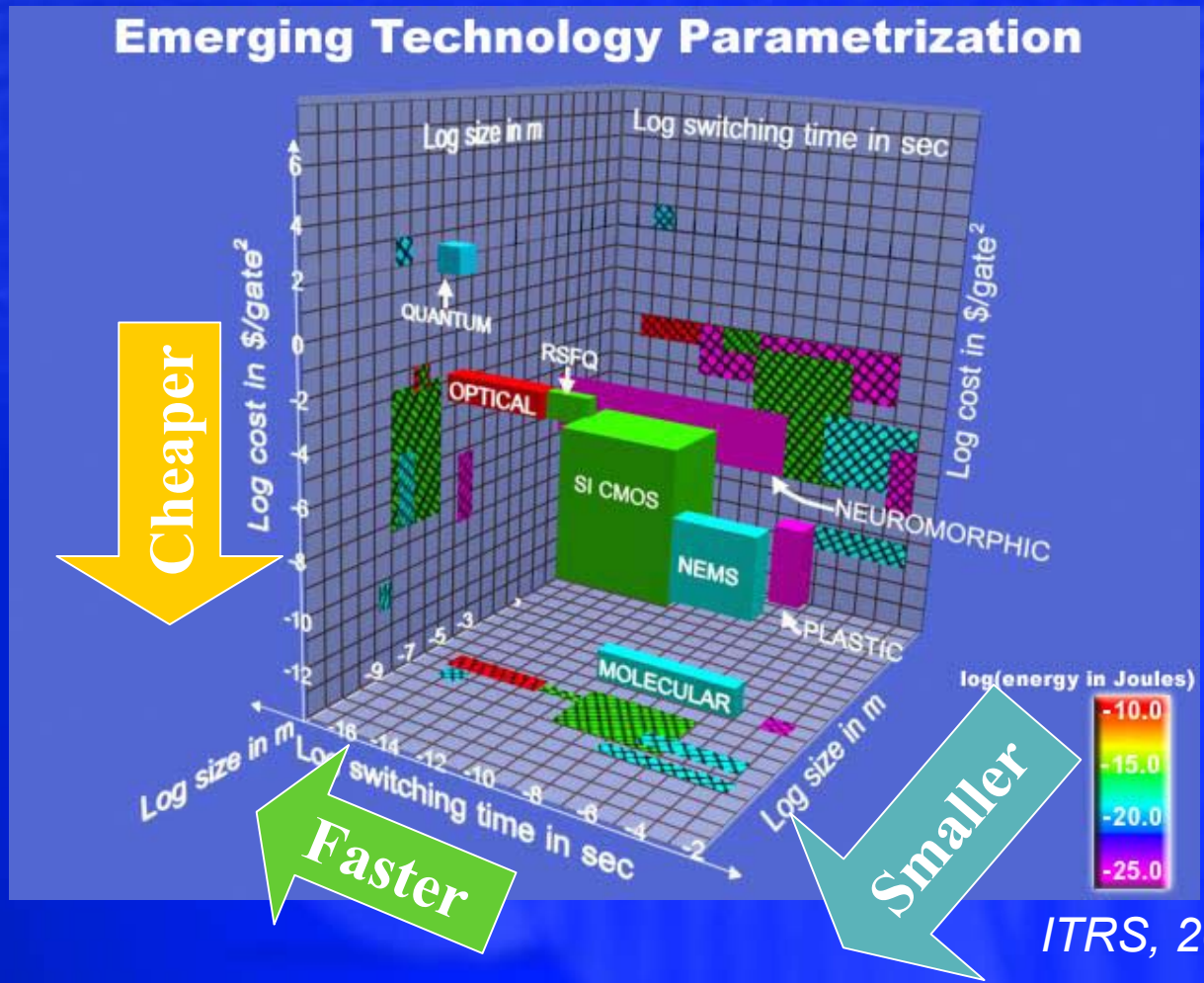
Some alternative logic devices



ITRS, 2001

Alternative logic devices exist which are complimentary to scaled silicon

Conclusions

- Intel's sub-100nm technology is already a production reality and continues to follow Moore's Law
- We believe the Silicon nanotechnology is extendable for at least 10 years
- Nanoscience research is needed to facilitate radical new scalable technologies for the future – we are open-minded about future options and collaborations between industries, universities and governments is essential

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For further information on Intel's silicon technology, please visit the Silicon Showcase at www.intel.com/research/silicon